REMARKS/ARGUMENTS

Interview Summary

Applicant thanks the Examiner for the opportunity to discuss the subject application on June 10, 2008. The inventor, Gord Allan, also participated in the interview. During the interview, Applicant explained in detail how at least the subject matter of claim 1 differed and should be patentable over the cited references. The Examiner was in tentative agreement at the end of the interview that claim 1 and its dependent claims might be patentable. The Examiner in a subsequent call to the undersigned indicated that he was reserving judgement on some of the other independent claims, such as claim 40 for example.

U.S.C 112 Rejections

In response to the claim rejection under 35 USC 112, claim 8 has been amended to depend upon claim 2. This results in there being a proper antecedent basis for the limitation "the control input(s)".

35 U.S.C 103 Rejections

Rejections based on combination of Iwamota with Saeki

The Examiner has rejected claims 1-12, 17, 18, 20-27, 30-38 as being unpatentable over Iwamoto (US 20020043996) in combination with Saeki (JP 57050391). To begin, it is noted that the remarks under this rejection also refer to claims 13 and 14. In the subsequent 35 U.S.C. 103 rejection relying on Matsuda, the Examiner explicitly concedes that the combination of Iwamoto and Saeki does not teach all of the limitations of claim 14. As such, in the response that follows, it is assumed that the Examiner intended to reject claims 1-13, 17,18 20-27 and 30-38 in the first obviousness rejection.

Iwamoto and Saeki are implementations of dual-direction digital-only shift registers using dynamic latches as the base storage element. As discrete shift-registers rather than analog integrators, they do not have either the mixed-signal or control characteristics of the claims 1-7,

23, 33. They are a fundamentally different approach to loop control than analog integrators, let alone a cascaded analog integrator as claimed.

Since the cited references, and similar art of this flavor, are digital, they do not have, anticipate, or require circuits that manipulate their analog characteristics (gain and frequency response), or require state retention as claimed in 8-17, 24-40.

Claim 1

As to claim 1, it recites "a plurality of mixed signal outputs." The Examiner submits that if Saeki's dynamic latches are substituted into Iwamoto's figure 5, that the outputs of Saeki's clocked inverters 21 and 22 form the mixed-signal outputs. In Iwamoto's figure 5, however, the back-to-back inverters 56/74, and 68/62 form positive feedback latches to prevent analog levels at the output nodes C(n). Iwamoto's use of these reconstruction elements is distinctly intended to prevent analog outputs, and therefore teaches away from their use.

Further, in Saeki's figure 1 (as in Iwamoto's figure 4), the outputs of the shifter circuit feed digital gates. Saeki's registers (1,2,3,4) Q outputs feed logic gates 5 and 6. Logic operations on analog levels are undefined, and if analog levels are maintained at the inputs to logic circuits, the excessive short-circuit currents may cause heating that may destroy the circuit. It appears this would prohibit Saeki from using steady-state analog levels at the output of the shifter.

Also with respect to claim 1, the Examiner contends that the Saeki/Iwamoto exhibit the claimed control states, to be paraphrased as 'integrate-up', 'integrate-dn', and 'hold'. During the active states in the claimed invention, based on claim 1 and figure 1 (100), it is clear that signal progression happens within a cell, and then successively into neighbouring cells for the duration of the state. Referring to Saeki's figure 5, the non-overlapping clocks phi1 and phi2 prevent sustained propagation during any state. This is critical in Saeki's case to maintain the master/slave relationship and for the device to operate as the intended shift-register. ie. to move one complete, but single, position for each pulse of the control signal. Other digital shifters suffer from the same restrictions and are fundamentally different than the claimed invention.

Claims 2-13, 17,18 and 20-22 all depend on claim 1 and should be allowable for the same

reasons. They describe the control (claim 2), are used to simplify the hardware (claims 3,4,7) manipulate the analog gain (5,6) frequency-response (8,9,12), reduce filter hardware by switching components to analog sections of the integrator (11) , and reduce power consumption (17). Claim 18 uses the circuit of claim 1 to control delay or frequency. As the combinations are unobvious, and make use of the unique structure and analog properties of the integrator of claim 1, the inventor submits that these combinations are also patentable.

Claim 2

As to dependent claim 2, as argued above, there is no equivalent shift left/right state in Saeki's reference. Saeki's control inputs L and R do nothing by themselves, and rather form the data select input to a shift-register. The clock signals phi1 and phi2 in figures 4 and 5 are the control inputs which define the following states, as in a conventional digital shifter:

Phi1	phi2	L/R	
0	0	x	hold
1	0	x	shift pre-charged data one stage (slave transparent)
0	1	L/R	master transparent with data-in from R/L neighbour

Claim 3

As to dependent claim 3, Saeki does not use a tri-state buffer as the unit cell. The pass transistor 24 prevents this.

Claim 4

As to dependent claim 4, Saeki does use a tri-state inverter as the driving cell, but it is gated by the transistor 24, unlike in claim 1 and dependent claim 4.

Claims 5 and 6

As to dependent claims 5 and 6, the logic on/off biasing circuits modulate the voltage to the gates, and thus the speed of the transistors responsible for charging/discharging. Transistors

31 and 34 in Saeki operate as switches and do not perform a similar function as in claims 5/6. More appropriately, the circuit of claim 5 could be used on the control inputs (phi and phibar) of Saeki's transistors 31 and 34 to regulate their speed, but this would adversely effect Saeki's circuit.

Claim 7

As to dependent claim 7, as Saeki's shift-register does not restrict the content of inputs 45 and 47 to VDD and VSS, each element in the chain (figure 3) must be capable of driving both up and down. This is unlike the claimed structure, where transistor pairs can be removed in alternate cells.

Claims 8 and 9

As to dependent claims 8 and 9, filtering in Saeki's reference (or similar) would increase power consumption, and degrade speed and performance. Because it is a digital circuit the filtering would have either no effect, or a detrimental effect on noise-immunity depending on the noise margin of the subsequent digital gates. Slowing the edge-rate with filtering in digital circuits degrades noise performance as it makes the gates susceptible to noise for a larger duty cycle. Unlike a digital shift-register, where slowing the edge rate is detrimental, the filtering in the analog integrator of claim 1 is a method used to control the loop dynamics.

Claims 10 – 13, 17, 24-27

As to the arguments against claims 10-12 and 17 since the shift-register of Saeki's figure 4 can be fed with arbitrary data at 45 and 47, there will not necessarily be a thermometer code in the shift-register. Even if certain input restrictions were applied to create such a thermometer code, the gate (43) in Saeki's figure 4 has no ability to sense or "dynamically determine" the transition point of such code or to use this information to perform useful tasks (as in claims 11-1-13, 25-27).

Claim 18

As to claim 18, a modified Iwamoto's figure 4 has a delay line only at 45, which is fed by

decode logic 43, neither of which can tolerate steady-state mixed-signal inputs.

Claim 20

As to claim 20, Iwamoto's figure 3 shows a delay locked loop circuit, but it does not use any form of analog integration. It is of the digital variety, where the delay is adjusted in a quantized step for each comparison cycle, rather than in an analog step proportional to the phase error. This is a fundamentally different type of DLL circuit.

Claim 21

As to claim 21, the phase locked loop circuit is accepted in the literature to contain an oscillator, and thus differentiates it from a DLL circuit. Iwamoto does not show a PLL.

Claim 22

As to claim 22, a deskew circuit is differentiated from a DLL circuit in that it introduces a delay which is not an integer multiple/sub-multiple of the clock period. Iwamoto does not show a deskew circuit.

Claims 23 to 27 and 30 to 32

Independent claim 23, and dependent claims 24 to 27 and 30 to 32 recognize that the method of analog integration within a cell and across into neighbouring cells is unique independent of the circuit of claim 1 and its corresponding dependents. For example, the method for determining the portions of the output which are analog in nature (by examining the neighbours – claims 24, 25, figure 15) is as novel as the circuit configuration that happens to perform the function (claim 10, figure 10a). Similar rationale applies to dependents 26, 27 and 30 to 32.

Claims 33 to 35

Independent claim 33, and its dependent claims 34 and 35, are derived from claim 1, 2 and 3, but recognize the usefulness of the structure without the 3rd 'hold' state. In this variation, the integrator is always 'active', either shifting-up or shifting-dn. As previously argued, as claim

1 has been shown to be patentable, this variation should also be patentable.

Claims 36 and 37

Independent claim 36 and dependent claim 37 describe how to recognize analog sections within a mixed-signal control code. This is non-trivial since potentially analog signals cannot be sent through conventional digital logic (to 'find' the analog section) without destructive and/or current-consuming short-circuit/constant currents. The proposed modified Iwamoto, has no method to determine where the transition point of the code is or use this information to perform useful functions. Iwamoto merely uses the output of the shift-register to insert the signal at a distinct point in the delay line 45. There is no method or need (because it is digital) to move components around to a certain point of the shift-register.

Claim 38

Dependent claim 38 the information referred to in the above discussion of claims 36 and 37, to connect filtering elements to analog nodes. The output of this circuit is a 'soft' indication of whether the node is analog, and the corresponding downstream logic is tolerant of this.

Rejections based on combination of Iwamota with Saeki and Matsuda

The Examiner further rejects claims 14-16, 27-29, 39-41 based on the combination of Iwamoto (US 20020043996) , Saeki (JP 57050391) and Matsuda (USP 5761134)

Matsuda is but one example of using a tri-stateable latch to hold digital state information. The applicant maintains that for some embodiments, the novelty is not in this, but in how to recognize where state-retention is necessary and connect devices appropriately.

Claims 14-16, 27-29

As to claims 14-16, 27-29 if the circuit in Saeki's figure 4 which generated phi1 and phi2 were gated off to save power, it appears that the tri-states would leak and state would be lost. Further, the circuitry of claim 14 permits state-storage despite having elements which can only drive uni-directionally (claim 7) to save area. The Examiner refers to the Masuda reference (USP

5,761,134), where a latch is capable of maintaining the digital output of a tri-state driver. The applicant accepts it as obvious that connecting a tri-state latch at each node of the circuit can be used to maintain the closest digital state. In the application of this circuit however, adding a latch at each output node for this purpose would more than double the active area of the design. The novelty of claims 14-16, and the associated circuitry in figure 10B is included at least in recognizing that only a small subset of nodes need active state retention, and in finding and connecting those nodes to a minimum number of state retention elements with minimal hardware. The applicant further submits that Iwamoto's circuitry 43, modified or not, has no capability to find either analog or digital transition points in a thermometer code and connect state retention elements applicably. In fact, the applicant notes that Iwamoto's all-digital circuit requires no such state-retention elements due to the reconstructive latches (which prohibit analog values and maintain digital ones) formed from inverter pairs 74/56 and 68/62.

Claim 19

As to claim 19, Iwamoto's figure 3 does not show or imply control of an LC oscillator. Merely having an inductive path (a wire) does not make an oscillator. Nevertheless, it may be considered that an extension of Iwamoto's work could be to control a switched bank LC oscillator with the shifter. This variant however, is not what is claimed in 19, since the control outputs of Iwamoto and similar art are digital – not analog or mixed-signal.

Claim 39

Dependent claim 39 the information referred to in the above discussion of claims 36 and 37, to connect state retention circuits to analog nodes. The output of this circuit is a 'soft' indication of whether the node is analog, and the corresponding downstream logic is tolerant of this.

Claims 40 and 41

Independent claim 40 and its dependent (41) are the complement to claim 36, where the method determines if a signal is clearly 'digital' in nature. This is not a simple inversion of the information gleaned from claim 36, since the output of circuit 36 is analog in nature. When a

signal is clearly digital, claim 41 is used to tie that signal to a voltage source and prevent loss of charge/voltage.

As to claim 40, all of potentially modified Iwamoto's outputs are digital. There is no circuitry that could detect and report on whether a node is analog or digital in nature (the latch of Saeki's inverters 21 and 22 is incapable of answering this question as it would be destructive to the original signal) nor is there any need of it in the references or similar art.

As to claim 41, all of potentially modified Iwamoto's outputs are digital, and state-retention elements are already inherent in the shifter which prevent charge leakage. There is no circuitry, or need of it, to find analog nodes or connect them to voltage sources.

Conclusion

The claimed staged analog integrator is a fundamentally different building block than a digital shifter. The analog circuit must be well controlled and deliver output step sizes proportional to the input signal duration. This does not occur in digital shifters, which move a quantized step for each input cycle.

The presented structure allows for a very efficient PLL or DLL because it can create an analog integrator and filter in a much smaller size than in a conventional (single stage) analog implementation. Since the invention moves in analog modulated steps (as opposed to digital methods), it avoids quantization induced problems and eliminates the need for digital signal-processing hardware to enforce stability.

In view of the foregoing, the Examiner is respectfully requested to withdraw the 35 U.S.C. 103 rejections of the claims. Early favourable consideration of this application is earnestly solicited.

Respectfully submitted,

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